

REMARKS

An Office Action was mailed March 3, 2009. This response is timely. Any fee due with this paper, including any necessary extension fees, may be charged on Deposit Account 50-1290.

Summary

Claims 1, 3, 11, 13, 21 and claims 25-27 are pending; other claims are cancelled or withdrawn.

Claims 1, 11, and 21 are the only independent claims.

By the foregoing, claims 1, 11, and 21 are amended. No new matter has been added.

35 U.S.C. §112, first paragraph

Claims 1, 3, 11, 13, 21 and 25-27 stand rejected under 35 U.S.C. §112, first paragraph as failing to be comply with the written description requirement. The claims have been amended and the rejection is respectfully rendered moot. Accordingly, the Examiner is respectfully requested to withdraw the rejection.

Rejection under 35 U.S.C. §102(b) and 35 U.S.C. §103(a)

claims 1, 3, 11, and 13 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,232,945 to Moriyama. Claims 25-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Moriyama in view of U.S. Patent No. 6,734,840 to Fukutofu. Independent claim 21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Moriyama in view of JP 2001-249643 to Hirobumi. Thus, all claims stand rejected at least over Moriyama.

All independent claims now claim that:

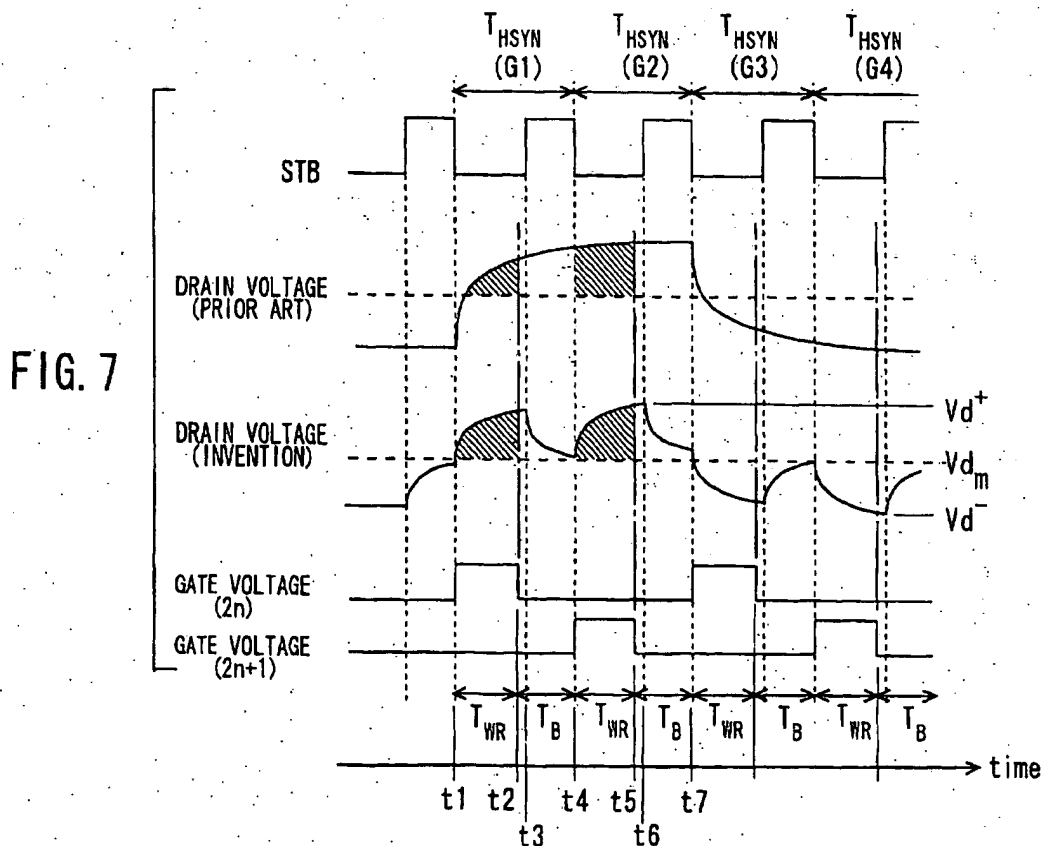
the source driver has a resetting means for resetting the data voltages outputted by the source driver circuit in a blanking period of each of the horizontal synchronizing periods of the set starting at an end of a writing period.

Support thereof may be found in the specification, as filed, on pg. 33, line 5 et al., and Fig.7

"the output of the shift register/latch circuit 141 is reset at the time t2 prior to the time t3. Therefore, the value of the data, voltage gradually decreases to its middle point voltage V_m . At the time t2, the pulse of the gate voltage (i.e., the selection voltage supplied from the gate driver circuit 13) falls. . . . As seen from FIG. 7, the period from t1 to t2 is the writing period T_{WR} while the period from t2 to t4 is the blanking period T_B . In this way, the resetting operation is carried out in the blanking period T_B .

The resetting circuit 142 is controlled in such a way that each of the data voltages will reach the middle point value V_- between the positive peak value V_+ and the negative peak value V_- after the resetting operation is completed. Here, the middle point value V_m is equal to the common voltage of the common electrode 24. " Emphasis added.

As Fig. 7 makes clear, the resetting occurs throughout the period t2 and t4, which corresponds to the blanking period, $T_{sub.B}$. This permits the entire blanking period to be used as a gradual voltage resetting operation is permitted.



Moriyama is cited for teaching a resetting circuit, which, as shown in Fig. 18, occurs in the blanking period.

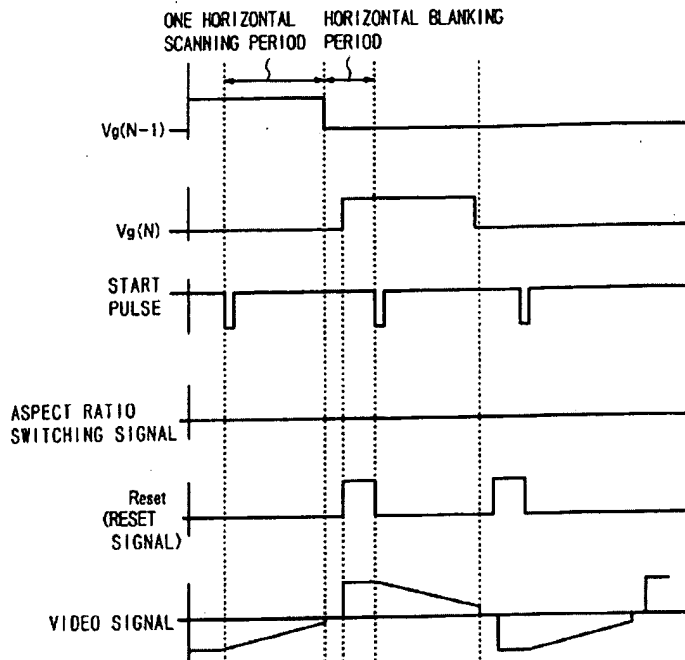


FIG. 18

However, the reset is offset from the horizontal scanning period. In the presently claimed invention, the resetting operation starts at the end of the writing, e.g., scanning, period.

The other cited art whether alone or in the combination with Moriyama as proposed does not teach, disclose, or suggest the claimed invention and the rejections are respectfully traversed for the reasons given.

In view of the remarks set forth above, this application is believed to be in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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